

**REMARKS**

The Official Action mailed August 24, 2005, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicants respectfully submit that this response is being timely filed.

The Applicants note with appreciation the consideration of the Information Disclosure Statements filed on July 24, 2003; and August 11, 2003.

Claims 1-4 and 11-14 were pending in the present application prior to the above amendment. Claim 2 has been amended to correct a minor typographical informality; and new dependent claims 15-22 have been added to recite additional protection to which the Applicants are entitled. Accordingly, claims 1-4 and 11-22 are now pending in the present application, of which claims 1, 2, 11 and 12 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraphs 3 and 4 of the Official Action rejects claims 1-4 as obvious based on the combination of JP 11-4001 to Yamazaki et al. and U.S. Patent No. 5,965,916 to Chen. The Applicants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in

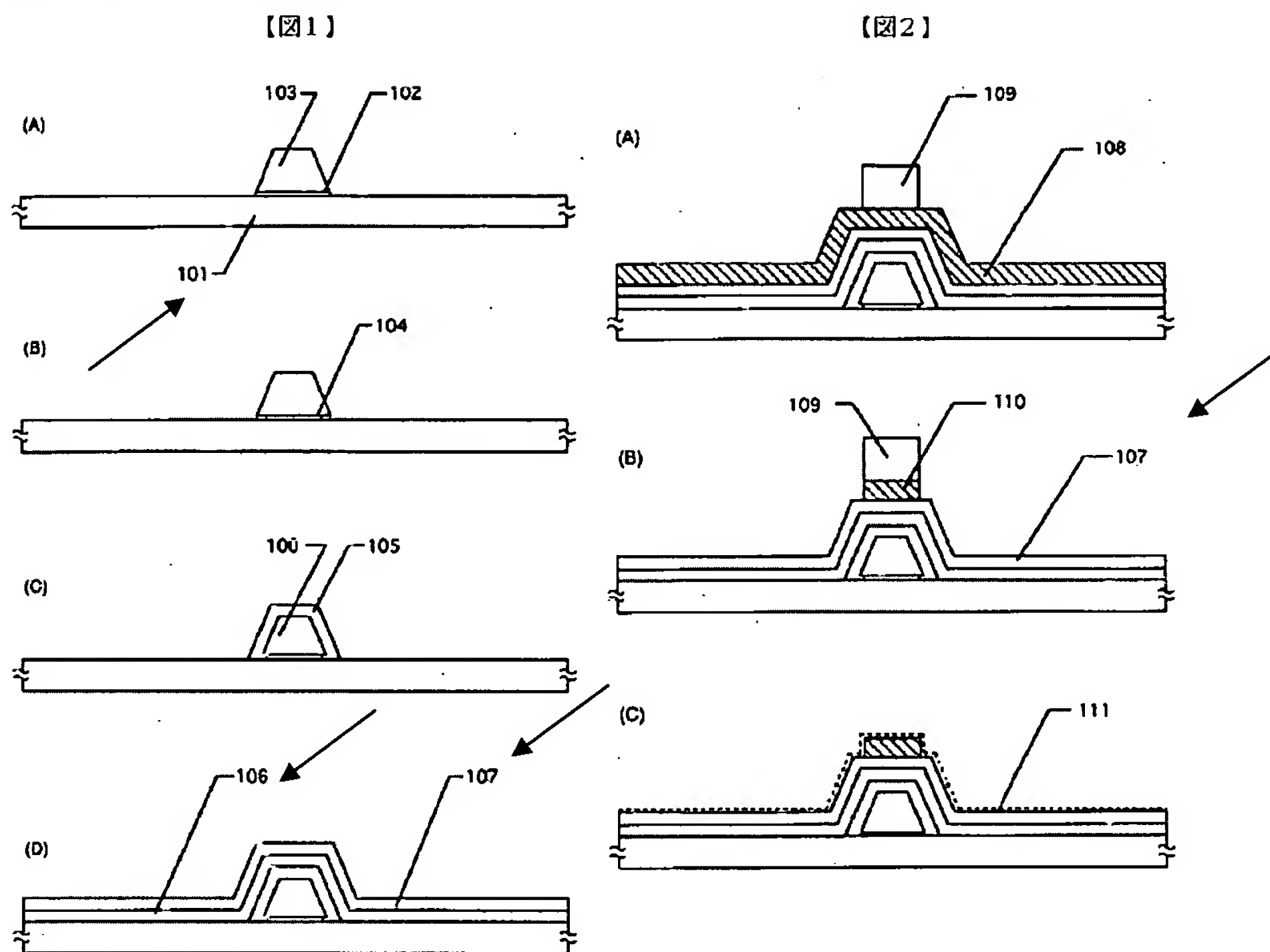
the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

There is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Yamazaki and Chen or to combine reference teachings to achieve the claimed invention. MPEP § 2142 states that the examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. It is respectfully submitted that the Official Action has failed to carry this burden. While the Official Action relies on various teachings of the cited prior art to disclose aspects of the claimed invention and asserts that these aspects could be modified in the manner asserted in the Official Action, it is submitted that the Official Action does not adequately set forth why one of skill in the art would combine the references to achieve the features of the present invention.

The test for obviousness is not whether the references "could have been" combined or modified as asserted in the Official Action, but rather whether the references should have been. As noted in MPEP § 2143.01, "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990) (emphasis in original). Thus, it is respectfully submitted that the standard set forth in the Official Action is improper to support a finding of *prima facie* obviousness.

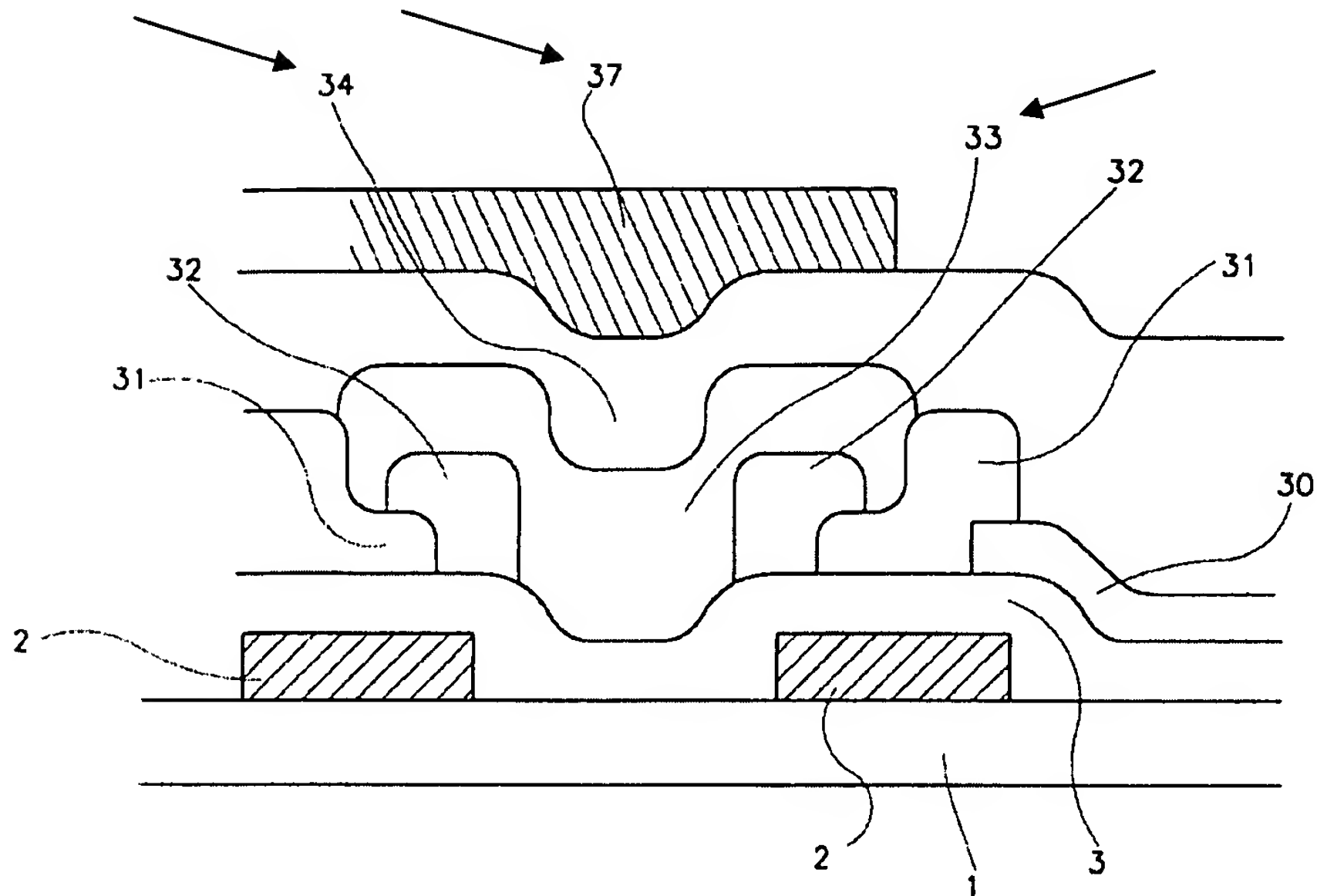
The Examiner relies on Yamazaki for the teaching of glass substrate 101, gate insulating film 106 and amorphous silicon film 107 and asserts that these features correspond with a light-transmitting substrate, a base film having a projection and an

island-like semiconductor layer, respectively, of the claims of the present application (page 2, Paper No. 20050822).



The Official Action concedes that Yamazaki "lacks anticipation of a gate insulating film over an island-like layer; and a gate electrode over the gate insulating film" (Id.). That is, the Official Action concedes that Yamazaki does not teach or suggest a gate electrode and a gate insulating film over amorphous silicon film 107.

The Official Action relies on Figure 6 of Chen for the teaching of gate metal layer 37, gate insulating layer 34 and a-Si layer 33 and asserts that these features correspond with the gate electrode, gate insulating film and island-like semiconductor layer, respectively, of the claims of the present application (page 3, Id.).



The Official Action does not identify whether the alleged combination of Yamazaki and Chen would involve replacing or somehow combining Yamazaki's amorphous silicon film 107 with Chen's a-Si layer 33. In any event, the Official Action asserts that one having ordinary skill in the art at the time the invention was made would have been motivated to modify Yamazaki's device by forming Chen's gate metal layer 37 and gate insulating layer 34 over Yamazaki's island-like layer 107 (or replacing Yamazaki's island-like layer 107 with Chen's a-Si layer 33) "since that would minimize display flicker as taught by Chen" (Id.). The Applicants respectfully disagree and traverse the above assertions in the Official Action.

Yamazaki is directed to a bottom gate type thin film transistor and teaches a gate electrode 100 under gate insulating film 106 as shown in Figures 1C and 1D (reproduced above). Yamazaki does not teach or suggest another type of thin film transistor such as a top gate type thin film transistor. That is, neither Yamazaki nor Chen teaches or suggests the removal or replacement of bottom gate 100 of Yamazaki. Please see U.S. Patent No. 6,501,094 to Yamazaki et al., which is of record and which is related to Yamazaki (JP 11-4001).

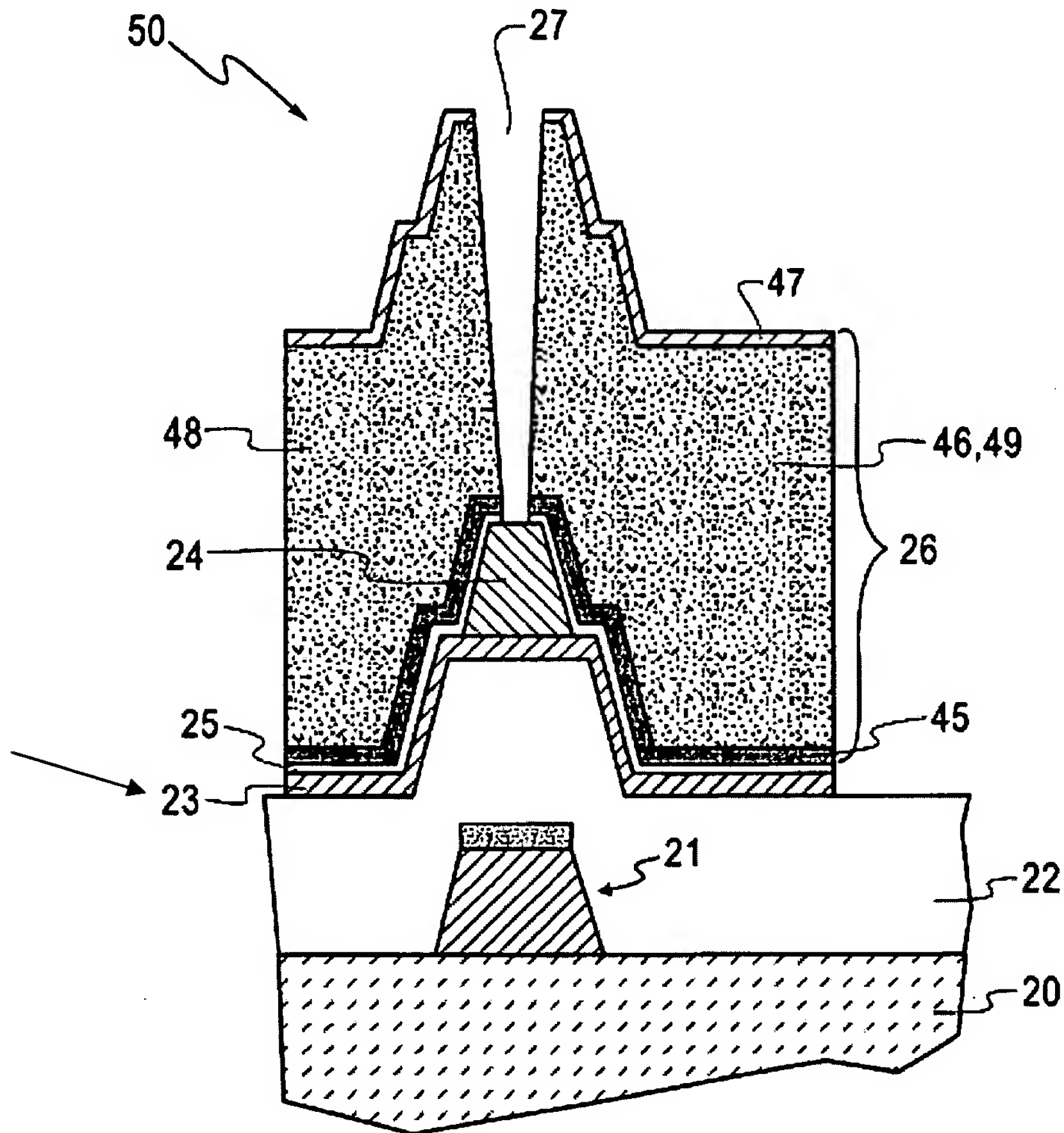
The Applicants note that the Official Action is relying on amorphous silicon film 107 to be "island-like" and the allegedly "island-like" feature of film 107 is apparently due to the fact that it is formed over gate 100. The alleged combination with Chen would either involve removing gate 100, which would remove the allegedly "island-like" feature of film 107, or would involve adding a second gate, which would render the resultant device inoperable.

Also, neither Yamazaki nor Chen teaches or suggests that Yamazaki's bottom gate type thin film transistor should be changed by forming Chen's gate metal layer 37 and gate insulating layer 34 over Yamazaki's amorphous silicon film 107 (or replacing Yamazaki's island-like layer 107 with Chen's a-Si layer 33). The alleged motivation to "minimize display flicker" appears to be briefly and very generally discussed in Chen at column 5, line 5 ("The invention also decreases the flicker of the display"). Chen does not teach or suggest that the minimization of display flicker is related to Chen's gate metal layer 37 and gate insulating layer 34, much less that this advantage would result if one were to form these particular features on an island-like semiconductor layer. Since the minimization of flicker is not related to Chen's gate metal layer 37 and gate insulating layer 34, it is not clear why one of ordinary skill in the art who was concerned with minimizing display flicker would not have simply practiced Chen alone, or would have gone out of their way to incorporate Chen's gate metal layer 37 and gate insulating layer 34 into Yamazaki's device.

Paragraphs 5 and 6 of the Official Action reject claims 11-14 as obvious based on the combination of U.S. Patent No. 6,258,723 to Takeichi et al. and Chen. The Applicants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

There is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Takeichi and Chen or to combine reference teachings to achieve the claimed invention.

Although not stated explicitly in the Official Action, it appears that the Official Action is asserting that a-Si:H layer 23 (Figure 5) corresponds with the island-like semiconductor layer of the claims of the present application.



**Fig. 5**

The rejection based on the alleged combination of Takeichi and Chen is similar to the alleged combination of Yamazaki and Chen in that the same motivation is asserted. The Official Action does not identify whether the alleged combination of Takeuchi and Chen would involve replacing or somehow combining Takeuchi's a-Si:H layer 23 with Chen's a-Si layer 33. In any event, the Official Action appears to assert



that one having ordinary skill in the art at the time the invention was made would have been motivated to modify Takeichi's device by forming Chen's gate metal layer 37 and gate insulating layer 34 over Takeichi's a-Si:H layer 23 (or replacing Takeichi's a-Si:H layer 23 with Chen's a-Si layer 33) "since that would minimize display flicker as taught by Chen" (page 6, Id.). The Applicants respectfully disagree and traverse the above assertions in the Official Action.

The Applicants respectfully submit that there is no motivation to combine Takeichi and Chen, because Takeichi is directed to a reverse staggered TFT and because Takeichi appears to teach a gate electrode 21 under a gate insulating film 22 as shown in Figure 5 (reproduced above). Further, it appears that Takeichi does not teach or suggest another type of thin film transistor such as a top gate type thin film transistor. That is, neither Takeichi nor Chen teaches or suggests the removal or replacement of the bottom gate of Takeichi.

The Applicants note that the Official Action is relying on a-Si:H layer 23 to be "island-like" and the allegedly "island-like" feature of a-Si:H layer 23 is apparently due to the fact that it is formed over gate electrode 21. The alleged combination with Chen would either involve removing gate electrode 21, which would remove the allegedly "island-like" feature of a-Si:H layer 23, or would involve adding a second gate, which would render the resultant device inoperable.

Also, please incorporate the arguments present above with respect to the deficiencies in Chen. For the reasons stated above, it is not clear why one of ordinary skill in the art who was concerned with minimizing display flicker would not have simply practiced Chen alone, or would have gone out of their way to incorporate Chen's gate metal layer 37 and gate insulating layer 34 into Takeichi's device.

Therefore, the Applicant respectfully submits that the Official Action has not provided a proper suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Yamazaki or Takeichi and Chen or to combine reference teachings to achieve the claimed invention.

In the present application, it is respectfully submitted that the prior art of record, either alone or in combination, does not expressly or impliedly suggest the claimed invention and the Official Action has not presented a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

For the reasons stated above, the Official Action has not formed a proper *prima facie* case of obviousness.

Furthermore, with respect to independent claims 11 and 12, the prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. Independent claims 11 and 12 recite that an island-like semiconductor layer is capable of being irradiated with light from another surface of a light-transmitting substrate through a region of a first thickness and a region of a second thickness. However, Takeichi's gate electrode 21 (or Chen's black matrix array 2) prevents semiconductor layer 23 from being irradiated with light from another surface of a light-transmitting substrate. Therefore, even if one were motivated to combine Takeichi and Chen, the prior art references do not teach or suggest the above-referenced features of the present invention. Since Takeichi and Chen do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained.

Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.



Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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